WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor construction assembly having a semiconductor substrate which has one surface, the other surface facing said one surface, and a plurality of side surfaces between said one surface and the other surface, and has an integrated circuit element formed on said one surface, a plurality of connection pads which are arranged on said one surface and connected to the integrated circuit element, a protective layer which is formed to cover said one surface of the semiconductor substrate and has openings for exposing the connection pads, and a plurality of conductors which are connected to the connection pads, arranged on the protective layer, and have pads;

an upper insulating layer which entirely covers said one surface of the semiconductor construction assembly including the conductors except the pads;

a sealing member which covers at least one side surface of the semiconductor construction assembly; and

upper conductors which are formed on the upper insulating layer, and has one ends electrically connected to the pads and an external connection pads, respectively, an external connection pad of at least one of the upper conductors being disposed in a region corresponding to the sealing member.

2. A semiconductor device according to claim 1,

wherein the sealing member covers an entire periphery of the semiconductor construction assembly.

3. A semiconductor device according to claim 1, wherein an insulating layer made of an inorganic material is formed between the semiconductor substrate and the protective layer of the semiconductor construction assembly.

4. A semiconductor device according to claim 1, wherein upper surfaces of the sealing member and the semiconductor construction assembly are flush with each other.

5. A semiconductor device according to claim 1, wherein lower surfaces of the sealing member and the semiconductor construction assembly are flush with each other.

6. A semiconductor device according to claim 1, wherein the semiconductor construction assembly has columnar electrodes formed on the conductors.

7. A semiconductor device according to claim 1, wherein the semiconductor construction assembly includes a sealing member formed between the columnar electrodes.

8. A semiconductor device according to claim 1, further comprising a base member which holds the semiconductor construction assembly and the sealing member.

9. A semiconductor device according to claim 8,

wherein the base member is made of a heat dissipation material.

10. A semiconductor device according to claim 8, further comprising an insulating layer which fixes the semiconductor construction assembly to the base member.

11. A semiconductor device according to claim 1, wherein the sealing member includes a buried member.

12. A semiconductor device according to claim 11, wherein the buried member has substantially the same thickness as a thickness of the semiconductor construction assembly.

13. A semiconductor device according to claim 11, wherein an insulating material is filled between the buried member and the semiconductor construction assembly.

14. A semiconductor device according to claim 1, wherein interlayer conductors which connect the conductors of the semiconductor construction assembly and the upper conductors, and an interlayer dielectric layer which covers the interlayer conductors are arranged between the upper conductors and the semiconductor construction assembly.

15. A semiconductor device according to claim 1, wherein an uppermost insulating layer is arranged on an upper surface of the dielectric layer including the upper conductors except the external connection pads of the upper conductors.

16. A semiconductor device according to claim 15, wherein projecting connection terminals are arranged on the external connection pads of the upper conductors.

17. A semiconductor device according to claim 16, wherein each of the projecting connection terminals includes a solder ball.

18. A semiconductor device according to claim 15, wherein an electronic component which is electrically connected to one of the external connection pads is arranged on the uppermost insulating layer.

19. A semiconductor device according to claim 15, wherein a connection pin is arranged on one of the external connection pads.

20. A semiconductor device according to claim 1, further comprising an electrical connection member which is electrically connected to one of the upper conductors, and extend through the sealing member to the other surface of the sealing member.

21. A semiconductor device according to claim 20, further comprising a conductor which is arranged on the other surface of the semiconductor construction assembly and connected to the electrical connection member.

22. A semiconductor device comprising:

a semiconductor construction assembly having a sealing member which covers one surface of a semiconductor substrate while externally exposing at least

an upper surface of a projecting electrode;

an upper insulating layer which covers one entire surface of the semiconductor construction assembly;

a sealing member which covers a side surface of the semiconductor construction assembly; and

an upper conductor which is formed on the upper insulating layer, electrically connected to the projecting electrode, and extends to a region corresponding to the sealing member.

23. A semiconductor device comprising:

a plurality of semiconductor construction assemblies each having an organic insulating film which covers one surface of a semiconductor substrate while externally exposing at least an upper surface of an electrode;

a sealing member which covers a side surface of each semiconductor construction assembly;

an upper insulating layer which covers one entire surface of each semiconductor construction assembly; and

one upper conductor which is formed on the upper insulating layer, electrically connected to at least one electrode, and extends to a region corresponding to the sealing member.

24. A semiconductor device comprising:

a first semiconductor device comprising a semiconductor construction assembly having an insulating

film which covers one surface of a semiconductor substrate while externally exposing at least upper surfaces of electrodes, a sealing member which covers a side surface of the semiconductor construction assembly, and upper conductors which are formed on the semiconductor construction assembly, electrically connected to the electrodes, and extend to a region corresponding to the sealing member; and

a second semiconductor device comprising a semiconductor construction assembly having an insulating film which covers one surface of a semiconductor substrate while externally exposing at least an upper surface of an electrode, a sealing member which covers a side surface of the semiconductor construction assembly, at least one upper conductor which is formed on the semiconductor construction assembly, electrically connected to the electrode, and extends to a region corresponding to the sealing member, and an electrical connection member which is arranged in the sealing member and connects the upper conductor to one of the upper conductors of the first semiconductor device.

25. A semiconductor device manufacturing method comprising:

arranging on a base plate a plurality of semiconductor construction assemblies in which a plurality of conductors having pads are formed on a semiconductor

substrate, so as to space apart the semiconductor construction assemblies from each other;

forming an insulating layer on an entire upper surface of the base plate including the plurality of semiconductor construction assemblies;

forming, on an upper surface of the insulating layer, upper conductors which have connection pads and are to be connected to corresponding pads of conductors of the semiconductor construction assemblies, so as to arrange at least one of the upper conductors on the insulating layer formed between the semiconductor construction assemblies; and

cutting the insulating layer between the semiconductor construction assemblies to obtain a plurality of semiconductor devices each having at least one semiconductor construction assembly in which the connection pad of the upper conductors is formed on the insulating layer in a region outside the semiconductor construction assembly.

26. A semiconductor device manufacturing method according to claim 25, wherein in cutting the insulating layer, the insulating layer is so cut as to contain a plurality of semiconductor construction assemblies.

27. A semiconductor device manufacturing method according to claim 25, wherein arranging the semiconductor construction assemblies on the base plate so

as to space apart the semiconductor construction assemblies from each other includes arranging a buried member between the semiconductor construction assemblies.

28. A semiconductor device manufacturing method according to claim 25, wherein the plurality of conductors are formed on a protective layer on the semiconductor substrate.

29. A semiconductor device manufacturing method according to claim 25, in which the insulating layer includes a plurality of layers, and which further comprises forming, between the layers, a plurality of interlayer conductors which connect conductors of the semiconductor construction assemblies and the upper conductors of corresponding sets.

30. A semiconductor device manufacturing method according to claim 25, further comprising forming an uppermost insulating layer on the upper surface of the insulating layer including the upper conductors except the pads of the upper conductors.

31. A semiconductor device manufacturing method according to claim 30, further comprising forming projecting connection terminals on the pads of the upper conductors.

32. A semiconductor device manufacturing method according to claim 31, wherein each of the projecting connection terminals includes a solder ball.

33. A semiconductor device manufacturing method according to claim 25, further comprising cutting the insulating layer and also cutting the base plate.

34. A semiconductor device manufacturing method according to claim 33, further comprising arranging another base plate below the base plate before cutting, and after cutting the base plate, removing said another base plate.

35. A semiconductor device manufacturing method according to claim 25, wherein arranging the semiconductor construction assemblies on the base plate so as to space apart the semiconductor construction assemblies from each other includes arranging a buried member between the semiconductor construction assemblies, and cutting the insulating layer between the semiconductor construction assemblies includes cutting the buried member.

36. A semiconductor device manufacturing method according to claim 35, wherein cutting the insulating layer between the semiconductor construction assemblies includes cutting the base plate.

37. A semiconductor device manufacturing method according to claim 25, further comprising removing the base plate before cutting the insulating layer between the semiconductor construction assemblies.

38. A semiconductor device manufacturing method according to claim 37, further comprising thinning the

semiconductor substrate subsequently to removing the base plate.